Comments of the
Semiconductor Industry Association

On

The Interim Final Rule Entitled
"Implementation of Additional Due Diligence Measures for Advanced Computing Integrated Circuits; Amendments and Clarifications; and Extension of Comment Period"

90 Fed. Reg. 5298 (January 16, 2025)
RIN 0694-AJ98
Docket No. 250108–0013

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The Semiconductor Industry Association (SIA) submits these comments in response to the request from the Bureau of Industry and Security (BIS) within the Department of Commerce (Commerce) in the interim final rule (IFR) entitled "Implementation of Additional Due Diligence Measures for Advanced Computing Integrated Circuits; Amendments and Clarifications; and Extension of Comment Period," 90 Fed. Reg. 5298.

Part I contains introductory and background comments about SIA and semiconductors and general comments about the IFR and the related semiconductor manufacturing and advanced computing rules in the Export Administration Regulations (EAR). Part II contains comments and questions regarding specific provisions in the IFR related to Foundry Due Diligence for BIS's consideration. Part III contains comments regarding specific provisions in the IFR that amended and clarified aspects of the interim final rule entitled "Foreign-Produced Direct Product Rule Additions, and Refinements to Controls for Advanced Computing and Semiconductor Manufacturing Items" (December 5 IFR).

Part I – Introduction and Background

SIA has been the voice of the U.S. semiconductor industry for almost 50 years. Our member companies represent more than 99% of the U.S. semiconductor industry by revenue and nearly two-thirds of non-U.S. firms, and are engaged in the full range of research, design, and manufacture of semiconductors – including both wafer fabrication and back-end assembly, test, and packaging of chips. Semiconductor technology was invented in America more than 65 years ago, and the U.S. remains the global leader in semiconductor technology and innovation, which drive America's economic strength, national security, and global competitiveness in a range of downstream industries. As stated by the President's Council of Advisors on Science and Technology, "It has never been clearer that leadership in semiconductors is a national priority to ensure both our

economic prosperity and our national security."[1] More information about SIA and the semiconductor industry is available at https://www.semiconductors.org/.

SIA and its member companies understand export controls are necessary tools for safeguarding national security. But these policies must be designed to avoid unduly harming commercial innovation, manufacturing, employment, and continued American leadership in critical technologies. As emphasized in our previous comment submissions,[2] the semiconductor industry encourages the U.S. government to align and implement U.S. export controls in a coordinated manner with other key supplier nations both to ensure the national security objectives of those actions are actually met and the U.S. semiconductor industry can compete on a level playing field around the world.

The U.S. export control regulations promulgated over the last few years are reshaping semiconductor supply chains and the global competitive landscape for chips and downstream chips-consuming firms alike, causing many customers around the globe to shift reliance to non-U.S. chips suppliers, and prompting retaliatory actions designed to degrade U.S. semiconductor competitiveness. At the same time, other governments have been aggressively negotiating market-opening trade deals to secure preferential access for their domestic companies and expand their economic influence and role in regional supply chains, while the U.S. has negotiated none – to the disadvantage of U.S. semiconductor companies and our global leadership.

We are encouraged by the comprehensive review that the Commerce Department and Office of the U.S. Trade Representative are undertaking to examine U.S. trade, economic security, and national security policies pursuant to President Trump's "America First Trade Policy" memorandum.[3] In the course of these reviews, we ask

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[1] President's Council of Advisors on Science and Technology, *Report to the President: Revitalizing the U.S. Semiconductor Ecosystem*, September 2022, https://bidenwhitehouse.archives.gov/wp-content/uploads/2022/09/PCAST_Semiconductors-Report_Sep2022.pdf.

[2] Comments of the Semiconductor Industry Association (SIA) on "Implementation of Additional Export Controls: Certain Advanced Computing Items; Supercomputer and Semiconductor End Use; Updates and Corrections; and Export Controls on Semiconductor Manufacturing Items; Corrections and Clarifications," (89 Fed. Reg. 23876 (April 4, 2024)), April 29, 2024, https://www.regulations.gov/comment/BIS-2023-0016-0036; Comments of the Semiconductor Industry Association (SIA) on "Implementation of Additional Export Controls: Certain Advanced Computing Items Supercomputer and Semiconductor End Use; Updates and Corrections," (88 Fed. Reg. 73458 (Oct. 25, 2023)), Jan. 17, 2024, https://www.regulations.gov/comment/BIS-2022-0025-0074; Comments of the Semiconductor Industry Association on "Export Controls on Semiconductor Manufacturing Items," (88 Fed. Reg. 73424 (Oct. 25, 2023)), Jan. 17, 2024, https://www.regulations.gov/comment/BIS-2023-0016-0015; Comments of the Semiconductor Association on "Foreign-Produced Direct Product Rule Additions, and Refinements to Controls for Advanced Computing and Semiconductor Manufacturing Items," (89 Fed. Reg 96790 (Dec. 2, 2024)), Feb. 28, 2025, https://www.semiconductors.org/wp-content/uploads/2025/02/SIA-Public-Comment-on-FDP-IFR.pdf.

[3] White House, "America First Trade Policy," January 20, 2025. https://www.whitehouse.gov/presidential-actions/2025/01/america-first-trade-policy/.

Trump Administration leadership to take into account the following points regarding the U.S. semiconductor industry:

- Roughly 70% of industry revenue comes from sales to overseas customers.
- We invest roughly 20% of revenue in R&D on average, among the most of any sector.
- SIA member companies are investing over half a trillion dollars in private capital in semiconductor production capacity in the U.S.
- Roughly two-thirds of U.S. headquartered front-end manufacturing facilities are located in the United States.

With respect to export control policy in particular, we ask Commerce Department leadership to undertake a comprehensive evaluation of past semiconductor-focused technology restrictions to determine whether they have achieved their specific national security and foreign policy objectives; understand the collateral impact on the U.S. national security innovation base — including the degree to which U.S. semiconductor technologies are "designed out" globally and replaced by foreign competitors not subject to U.S. export controls jurisdiction or similar export control regimes ; and work together with other relevant agencies to assess whether other policy tools may be more effective.

We also urge the Commerce Department and other key agencies involved in developing and implementing export controls to consider appropriate mechanisms for facilitating engagement with the private sector in the policymaking process. SIA member companies have extensive market and technical expertise to bring to bear. In past comments, we have encouraged the Commerce Department to re-establish the President's Export Council Subcommittee on Export Administration (PECSEA), which the previous Administration had promised but failed to deliver.[4] We also support review of the BIS Technical Advisory Committees (TACs) and updating the membership of the TACs.

SIA has long been a partner of the U.S. government in providing constructive and substantive feedback to ensure semiconductor technology and related controls are crafted in a manner that enhances our national security and have straightforward compliance obligations, while still enabling SIA member companies to out-compete, out-innovate, and win the competition for global semiconductor leadership.

We appreciate the opportunity to provide comments and questions with respect to the IFR, and request that BIS swiftly publish FAQs to clarify key technical details and reduce regulatory uncertainty regarding specific provisions in the IFR, as identified in the forgoing comments. Given that the IFR includes separate provisions on "Implementation of Additional Due Diligence Measures for Advanced Computing

[4] Bureau of Industry and Security, "Notice of Reestablishment of the President's Export Council Subcommittee on Export Administration and Solicitation of Nominations for Membership," 89 Fed. Reg 1064 (Jan. 9, 2024), https://www.federalregister.gov/documents/2024/01/09/2024-00190/notice-of-reestablishment-of-the-presidents-export-council-subcommittee-on-export-administration-and.

Integrated Circuits" and "Amendments and Clarifications" to the December 5 IFR,[5] we have grouped our comments accordingly.

Part II – Comments on Provisions related to Foundry Due Diligence in the IFR

SIA provides comments on several provisions and technical details in the IFR on which we seek clarification and revision.

In October 2023, BIS published an interim final rule entitled "Implementation of Additional Export Controls: Certain Advanced Computing Items; Supercomputer and Semiconductor End Use; Updates and Corrections," imposing controls on integrated circuits (ICs) that are critical for advanced computing and AI applications (AC/S IFR). The AC/S IFR established Red Flags and due diligence requirements to assist "front-end fabricators" when evaluating information provided by IC designers as to IC performance capabilities and assess whether foreign parties may be attempting to circumvent controls. According to the preamble of the January 16 IFR, Red Flag 19 outlined specific factors to identify a potential advanced computing IC, and explained "that if the item that would be produced is an IC, or a computer, "electronic assembly," or "component" that incorporates more than 50 billion transistors and high bandwidth memory (HBM), it raises a Red Flag that there is a high degree of likelihood that a license is required under the EAR."

The January 16 IFR explains that BIS has since assessed that "ICs with a transistor count below that specified in current Red Flag 19 (50 billion) can meet the performance threshold specified in ECCN 3A090." The preamble to the January 16 IFR further discusses scenarios where a foundry does not control the final packaging of an IC, and where a customer "may request an IC with a transistor count just below the current [50 billion] transistor count Red Flag threshold, and contract with an outsourced semiconductor assembly and test company ("OSAT") to incorporate that IC into a packaged item that exceeds the performance thresholds specified in ECCN 3A090."

In response to these concerns, the January 16 IFR imposes a broader license requirement for both front end fabricators and OSATs. Note 1 to ECCN 3A090.a. requires that a front-end fabricator or OSAT seeking to supply any logic IC produced using the 16/14 nanometer node or below or using a non-planer transistor architecture (applicable advanced logic integrated circuits), must presume the IC is controlled under 3A090.a. and designed or marketed for datacenters unless this presumption can be overcome in one of three specified ways. The presumption can be overcome by (i) an attestation by an "approved" or "authorized" IC designer, (ii) an attestation by a front-end fabricator located outside of Macau or a Country Group D:5 destination or (iii) an

[5] Bureau of Industry and Security, "Foreign-Produced Direct Product Rule Additions and Refinements to Controls for Advanced Computing and Semiconductor Manufacturing Items," 89 Fed. Reg 96790 (Dec. 5, 2024), https://www.govinfo.gov/content/pkg/FR-2024-12-05/pdf/2024-28270.pdf.

attestation by an "approved" OSAT. EAR 742.6(a)(6)(iii)(A) requires a license for supply of items classified under ECCN 3A090.a worldwide.

Comment II.A: BIS should consider establishing an exemption to the Note 1 to 3A090.a. requirements for ICs below a certain transistor count.

We request BIS consider establishing an exemption to the Note 1 requirements for ICs with less than ten billion transistors, given that these ICs are substantially below the red flag threshold and unlikely to be used in AI training, which we understand to be the primary national security concern motivating these controls.

The IFR is focused on limiting shipments of ICs that contain more than 30 billion transistors and are packaged with HBM. There is a significant delta between these identified performance thresholds that trigger national security concerns and typical commercial chips. If BIS is concerned about ICs incorporating less than 10 billion transistors that are packaged with HBM, we suggest that BIS limit the above request to ICs incorporating less than 10 billion transistors that do not contain HBM or HBM equivalent capability (e.g., die-to-die connection).

Comment II.B: BIS should exempt "multi-project wafers" from the Note 1 to 3A090.a requirements.

"Multi-project wafers" (MPWs) are used by front-end fabricators to facilitate semiconductor IP validation or to make prototypes to validate customer's semiconductor design. They are usually shipped in singular die form (after bumping and dicing) or in wafer form. MPW chips are generally produced in small volume (a few hundred dies per batch for each design) and the transistor count of each die is fixed after bumping and dicing processes by the front-end fabricator, thereby minimizing the risk of the dies being packaged into a more powerful chip later. Typically, multiple IC designs may be included in a single "shuttle," which allows multiple customers to share the cost of wafer fabrication for prototypes or low-volume production runs. The low volume and transistor count of the ICs included in the MPW wafers makes them insufficient to support AI applications. As written, the IFR imposes substantial regulatory burden for each MPW submission.

We therefore request BIS exempt such ICs from the above requirements given the chips present no national security concern and are not intended to be governed by this IFR. Specifically, we request that either BIS carve out MPW chips from the scope of requirements under current IFR, or alternatively accept an attestation by front-end fabricators that an "applicable advanced logic integrated circuit" has fewer than 30 billion transistors as sufficient to overcome a presumption that the IC is controlled under 3A090.a. If BIS still considers a certain level of control over such ICs necessary, we recommend BIS establish an upper threshold of 600 bare dies or 10 wafers per shuttle per single end user for an exception from the approved OSAT requirements.

Comment II.C: BIS should exempt test chips produced by a front-end fabricator for the purposes of testing or verifying its own processes from the Note 1 to 3A090.a presumption.

We propose that test chips produced by a front-end fabricator for the purposes of testing or verifying its own processes should be exempt from the 3A090.a presumption even if such chips may need to be shipped to an approved OSAT for packaging before being returned to the front-end fabricator. Such test chips are intended solely for the internal use of the front-end fabricator and do not possess the function of products produced for the front-end fabricator's customers. Therefore, such test chips should not be covered by the presumption in Note 1 to 3A090.a.

We request that BIS revise Note 1 to 3A090.a to include the following (changes indicated in bold):

> ***Note 1 to 3A090.a****: When a "front-end fabricator" or "OSAT" company is seeking to export, reexport, or transfer (in-country) an "applicable advanced logic integrated circuit," there is a presumption that the item is 3A090.a and designed or marketed for datacenters. If the "front-end fabricator" or "OSAT" company cannot overcome this presumption, then it must comply with all license requirements applicable to items specified in 3A090.a. However, this presumption does not apply to any entity other than the "front-end fabricator" or "OSAT" company.* ***Test wafers for the sole purposes of testing or verifying "front-end fabricator" company's own processes and are returned to the front-end fabricator after OSAT's packaging are excluded from this presumption****. A "front-end fabricator" or "OSAT" company can overcome this presumption in any of the following three ways outlined in paragraphs a. through c. of this Note 1.*

Comment II.D: BIS should exempt a front-end fabricator from the requirement to obtain an attestation from the approved OSAT, where the front-end fabricator is shipping to the approved OSAT.

Note 1 to ECCN 3A090.a requires a front-end fabricator to have an approved OSAT's attestation before the front-end fabricator can ship to the approved OSAT (in cases where the IC designer is neither approved nor authorized). However, this requirement creates certain practical operational challenges.

At the time a front-end fabricator ships the wafer to an approved OSAT, the product is not yet in its final packaged form. Therefore, an attestation provided by the approved OSAT would be based on the final package design planned for production, not the final packaged product. As such, it is impossible for an OSAT to provide an accurate attestation to the front-end fabricator on the "final packaged IC" before receiving the actual product and examining the final packaged IC, and without technical details provided by the front-end fabricator.

Comment II.E: BIS should expressly exclude "dummy" transistors from the Note 1 to 3A090.a requirements.

Note 1 to 3A090.a does not include any guidance on whether so-called "dummy" transistors should be counted. These dummy transistors are non-functional and do not contribute to logic performance. Rather, they are merely incorporated into the layout to ensure that subsequent processes, such as photolithography, etching and further chemical mechanical polishing occur uniformly over all segments. The use of dummy transistors is a standard industry practice to increase yield and minimize defects. We BIS should clarify the rule to expressly exclude these dummy transistors when counting the number of transistors in terms of the threshold of 30 billion transistors for overcoming the 3A090.a presumption.

Comment II.F: Wholly owned subsidiaries of U.S. companies should be included as approved IC designers or approved OSATs if their parent company receives this designation, regardless of their location.

To apply to be added to the list of approved OSATs, EAR Part 748.16 specifies that an OSAT must submit a request in the form of an advisory opinion to BIS, and the processing of the advisory opinion request will follow the interagency process for review of Validated End-User requests set forth in supplement no. 9 to part 748 of the EAR. The rule does not specify whether a subsidiary of an approved OSAT also constitutes an approved OSAT.

The U.S. parent company of a wholly owned foreign subsidiary is ultimately responsible for the due diligence required to meet the standards set for designation as an approved IC designer or an approved OSAT. Should a wholly owned foreign subsidiary of U.S. parent company be unable to receive designation as an approved OSAT company under this framework, foreign OSATs will simply backfill the business that is lost, creating a competitive disadvantage and not addressing the national security objectives articulated in the IFR.

We therefore request BIS to revise this rule to clarify that all subsidiaries of approved OSATs are also approved OSATs. If BIS determines not all subsidiaries of approved OSATs qualify as approved OSATs, we request BIS revise the rule to make clear that where a packaging site of an approved OSAT provider located in a D:5 country is packaging and shipping applicable advanced logic ICs, an attestation provided by the parent who is an approved OSAT is sufficient to overcome the presumption in Note 1 to 3A090.a.

Comment II.G: BIS should amend the rule to harmonize the definition of OSAT in § 772.1 and the § 748.16 requirements on becoming an approved OSAT.

The IFR adds a new definition of OSAT in § 772.1. An OSAT is defined as a company responsible for "assembling, packaging, **and** testing ICs and other semiconductor devices."

However, § 748.16, which outlines the process for becoming an approved OSAT or integrated circuit designer currently states that only entities that have "designed, assembled, tested, **or** packaged ICs will be considered for addition to the Approved OSAT or Approved Integrated Circuit Designers Lists." In practice, the data validation on the IC transistor count can only be done by the party doing the packaging/assembly work and could not be done by an entity just providing test services. Thus, the OSAT attestation should come at the packaging step, rather than being left ambiguous.

We request that BIS revise § 748.16 to include the following:

> "***Only entities that have designed integrated circuits, or packaged/assembled integrated circuits, will be considered for addition to either list****."*

Part III: Comments on "Amendments and Clarifications" to the December 5 IFR

Comment III.A: BIS should revise the text of ECCN 3D992.b to accurately reflect the regulatory intent expressed in the IFR's preamble, thus correcting a technical drafting error in which the term, "specially designed" was omitted.

The scope of ECCN 3D992 is described in the preamble of the January 16 IFR as follows:

> *c. Revisions to ECCNs **3D992**, 3D993, 3D994, 3E992, 3E993, and 3E994. Paragraphs 3D992.a, 3D993.a, 3E993.a are **amended by adding "specially designed" for consistency with other 990 series software controls**. ECCNs 3D994 and 3E994 are amended by adding "specially designed" to the heading for consistency with other 990 series software and technology controls.*

However, the text of ECCN 3D992.b on the CCL does not reflect the preamble of the IFR. As a result, ECCN 3D992.b is overly broad and can be interpreted to include software already controlled under other entries, such as ECCN 3D001 and 3D991. Without the amendment for inclusion of "specially designed", ECCN 3D992.b is ambiguous and could control non-electronic design automation software, such as computer aided design software and general-purpose solvers for consumer electronics. This conflict between the text of ECCN 3D992.b and the preamble appears contrary to the rulemaking requirements of the Export Control Reform Act, as recounted by BIS in the IFR:

> *. . . as noted under § 1752(7) of ECRA, administering export controls in an effective manner "**requires a clear understanding both inside and outside the U.S. Government of which items are controlled**."*

We therefore recommend that BIS publish the following revised text for ECCN 3D992.b so that it is consistent with the intent of the control as described in the preamble (change indicated in bold):

> *b. 'Electronic Computer-Aided Design' ('ECAD') "software"* ***"specially designed"*** *for the integration of multiple dies into a 'multi-chip' integrated circuit, and having all of the following:*
>
> *b.1. Floor planning; and*
>
> *b.2. Co-design or co-simulation of die and package.*
>
> *Technical Note: For the purposes of 3D992.b, 'multi-chip' includes multi-die and multi-chiplet.*

In the interim, we respectfully request that BIS issue a Frequently Asked Question on the scope of ECCN 3D992.b so that the exporting public is aware that the text should be interpreted in accordance with the preamble of the IFR.

* * *

Thank you for the opportunity to comment on the IFR. SIA looks forward to continued partnership with BIS and other agencies in providing support and feedback regarding export control policy, particularly with respect to semiconductors.

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